M16C/62P, M32C/84 Group

Differences between M16C/62P and M32C/84

1. Abstract

The following document describes differences between M16C/62P 128-pin version and M32C/84 144-pin version. Refer to each device's hardware manual or software manual for details.

2. Introduction

The explanation of this issue is applied to the following condition:
Applicable MCU: M16C/62P 128-pin version, M32C/84 144-pin version

3. Differences Outline

3.1 Differences Outline of Functions

Table 3.1.1 lists the differences of functions.

Table 3.1.1 Differences of Functions (1)

Item	M16C/62P	M32C/84
Basic Instructions	91 instructions	108 instructions
Minimum Instruction Execution Time	41.7ns(f(BCLK) = 24MHz, VCC1 = 3.0 V to 5.5 V) 100ns(f(BCLK) = 10MHz, VCC1 = 2.7 V to 5.5 V)	31.3ns(f(BCLK) = 32MHz, VCC1 = 4.2 V to 5.5 V) 41.7ns(f(BCLK) = 24MHz, VCC1 = 3.0 V to 5.5 V)
Address Space	1-Mbyte (Available to 4 Mbytes by memory space expansion function)	16-Mbyte
I/O Port	I/O Port: 113, Input Port: 1	I/O Port: 123, Input Port: 1
Intelligent I/O	N/A	Time measurement function: 16 bits x 8 channels Waveform generating function: 16 bits x 8 channels Communication function (Clock synchronous serial I/O, Clock asynchronous serial I/O, HDLC data processing)
Serial Interface	3 channels Clock synchronous serial I/O Clock asynchronous serial I/O I^2C bus, IEBus(2) 2 channels Clock synchronous serial I/O	5 channels Clock synchronous serial I/O Clock asynchronous serial I/O I^2C bus IEBus (optional) (2) (3)
CAN Module	N/A	1 channels
A/D Converter	10-bit A/D converter: 1 circuit, 26 channels	10-bit A/D converter: 1 circuit, 34 channels
DMAC	2 channels	4 channels
DMAC II	N/A	Available
X/Y Converter	N/A	16 bits x 16 bits
Interrupt	29 internal and 8 external sources, 4 software sources	38 internal and 8 external sources, 5 software sources
Oscillation Stop Detect Function	Stop detection of main clock oscillation, re-oscillation detection function	Stop detection of main clock oscillation
Supply Voltage	VCC1 = 3.0 V to 5.5 V, VCC2 = 2.7 V toVCC1 (f(BCLK) = 24MHz) VCC1 = 2.7 V to 5.5 V, VCC2 = 2.7 V to VCC1 (f(BCLK) = 10MHz)	VCC1 = 4.2 V to 5.5 V, VCC2 = 3.0 V to VCC1 (f(BCLK) = 32MHz) VCC1 = 3.0 V to 5.5 V, VCC2 = 3.0 V to VCC1 (f(BCLK) = 24MHz)
Power Consumption	14mA(VCC1 = VCC2 = 5 V, f(BCLK) = 24MHz) 8mA(VCC1 = VCC2 = 3 V, f(BCLK) = 10MHz) 2.0μA(VCC1 = VCC2 = 5 V, f(XCIN) = 32kHz, wait mode) 0.8μA(VCC1 = VCC2 = 5 V, stop mode)	28mA(VCC1 = VCC2 = 5 V, f(BCLK) = 32MHz) 22mA(VCC1 = VCC2 = 3.3 V, f(BCLK) = 24MHz) 10μA(VCC1 = VCC2 = 5 V, f(BCLK) = 32kHz, wait mode) 0.8μA(VCC1 = VCC2 = 5 V, stop mode)
Program and Erase Endurance	100 times (all area) or 1,000 times (user ROM area without block A and block 1) / 10,000 times (block A, block 1)	100 times (all area)

NOTES:
1. Refer to hardware manual for Electrical Characteristics and details.
2. IEBus is a trademark of NEC Electronics Corporation.
3. Please contact a Renesas sales office for optional features.

3.2 Differences of Pin Characteristics

Tables 3.2.1 and 3.2.2 list the differences of pin characteristics.

Table 3.2.1 Differences of Pin Characteristics (1/2)

M16C/62P	M32C/84	Differences from M16C/62P
P9_7/SIN4/$\overline{\text{ADTRG}}$	P9_7/RXD4/SCL4/STXD4/$\overline{\text{ADTRG}}$	Add RXD4/SCL4/STXD4 Delete SIN4
P9_6/SOUT4/ANEX1	P9_6/TXD4/SDA4/SRXD4/ ANEX1	Add TXD4/SDA4/SRXD4 Delete SOUT4
P9_4/TB4IN/DA1	P9_4/TB4IN/$\overline{\text{CTS4}}$/$\overline{\text{RTS4}}$/$\overline{\text{SS4}}$/DA1	Add $\overline{\text{CTS4}}$/$\overline{\text{RTS4}}$/$\overline{\text{SS4}}$
P9_3/TB3IN/DA0	P9_3/TB3IN/$\overline{\text{CTS3}}$/$\overline{\text{RTS3}}$/$\overline{\text{SS3}}$/DA0	Add $\overline{\text{CTS3}}$/$\overline{\text{RTS3}}$/$\overline{\text{SS3}}$
P9_2/TB2IN/SOUT3	P9_2/TB2IN/TXD3/SDA3/SRXD3	Add TXD3/SDA3/SRXD3 Delete SOUT3
P9_1/TB1IN/SIN3	P9_1/TB1IN/RXD3/SCL3/STXD3	Add RXD3/SCL3/STXD3 Delete SIN3
P14_1	P14_1/INPC1_5/OUTC1_5	Add INPC1_5/OUTC1_5
P14_0	P14_0/INPC1_4/OUTC1_4	Add INPC1_4/OUTC1_4
P8_4/$\overline{\text{INT2}}$/ZP	P8_4/$\overline{\text{INT2}}$	ZP is shared with $\overline{\text{INT2}}$
P8_3/$\overline{\text{INT1}}$	P8_3/$\overline{\text{INT1}}$/CAN0IN	Add CAN0IN
P8_2/$\overline{\text{INT0}}$	P8_2/$\overline{\text{INT0}}$/CAN0OUT	Add CAN0OUT
P8_1/TA4IN/$\overline{\text{U}}$	P8_1/TA4IN/$\overline{\text{U}}$/INPC1_5/OUTC1_5	Add INPC1_5/OUTC1_5
P8_0/TA4OUT/U	P8_0/TA4OUT/U/ISRXD0	Add ISRXD0
P7_7/TA3IN	P7_7/TA3IN/CAN0IN/INPC1_4/OUTC1_4/ISCLK0	Add CAN0IN/INPC1_4/OUTC1_4/ISCLK0
P7_6/TA3OUT	P7_6/TA3OUT/ CAN0OUT/INPC1_3/ OUTC1_3/ISTXD0	Add CAN0OUT/INPC1_3/OUTC1_3/ISTXD0
P7_5/TA2IN/$\overline{\text{W}}$	P7_5/TA2IN/$\overline{\text{W}}$/INPC1_2/OUTC1_2/ISRXD1/BE1IN	Add INPC1_2/OUTC1_2/ISRXD1/BE1IN
P7_4/TA2OUT/W	P7_4/TA2OUT/W/ INPC1_1/OUTC1_1/ISCLK1	Add INPC1_1/OUTC1_1/ISCLK1
P7_3/TA1IN/$\overline{\text{V}}$/$\overline{\text{CTS2}}$/$\overline{\text{RTS2}}$	P7_3/TA1IN/$\overline{\text{V}}$/$\overline{\text{CTS2}}$/$\overline{\text{RTS2}}$/$\overline{\text{SS2}}$/INPC1_0/ OUTC1_0/ISTXD1/BE1OUT	Add $\overline{\text{SS2}}$/INPC1_0/OUTC1_0/ISTXD1/BE1OUT
P7_1/TA0IN/TB5IN/RXD2/SCL2	P7_1/TB5IN/TA0IN/RXD2/SCL2/STXD2/ INPC1_7/OUTC1_7	Add STXD2/INPC1_7/OUTC1_7/
P7_0/TA0OUT/TXD2/SDA2	P7_0/TA0OUT/TXD2/SDA2/SRXD2/ INPC1_6/OUTC1_6	Add SRXD2/INPC1_6/OUTC1_6
P6_7/TXD1/SDA1	P6_7/TXD1/SDA1/SRXD1	Add SRXD1
P6_6/RXD1/SCL1	P6_6/RXD1/SCL1/STXD1	Add STXD1
P6_4/$\overline{\text{CTS1}}$/$\overline{\text{RTS1}}$/$\overline{\text{CTS0}}$/CLKS1	P6_4/$\overline{\text{CTS1}}$/$\overline{\text{RTS1}}$/$\overline{\text{SS1}}$	Add $\overline{\text{SS1}}$ Delete $\overline{\text{CTS0}}$/CLKS1
P6_3/TXD0/SDA0	P6_3/TXD0/SDA0/SRXD0	Add SRXD0
P6_2/RXD0/SCL0	P6_2/RXD0/SCL0/STXD0	Add STXD0
P6_0/$\overline{\text{CTS0}}$/$\overline{\text{RTS0}}$	P6_0//$\overline{\text{CTS0}}$/$\overline{\text{RTS0}}$/$\overline{\text{SS0}}$	Add $\overline{\text{SS0}}$
P5_7/$\overline{\text{RDY}}$/CLKOUT	P5_7/$\overline{\text{RDY}}$	Delete CLKOUT
P5_4/$\overline{\text{HLDA}}$	P5_4/$\overline{\text{HLDA}}$/ALE	Add ALE
P5_3/BCLK	P5_3/CLKOUT/BCLK/ALE	Add CLKOUT/ALE
P4_7/$\overline{\text{CS3}}$	P4_7/$\overline{\text{CS0}}$/A23	Add $\overline{\text{CS0}}$/A23 Delete $\overline{\text{CS3}}$
P4_6/$\overline{\text{CS2}}$	P4_6/$\overline{\text{CS1}}$/A22	Add $\overline{\text{CS1}}$/A22 Delete $\overline{\text{CS2}}$
P4_5/$\overline{\text{CS1}}$	P4_5/$\overline{\text{CS2}}$/A21	Add $\overline{\text{CS2}}$/A21 Delete $\overline{\text{CS1}}$
P4_4/$\overline{\text{CS0}}$	P4_4/$\overline{\text{CS3}}$/A20	Add $\overline{\text{CS3}}$/A20 Delete $\overline{\text{CS0}}$
P3_7/A15	P3_7/A15(/D15)	Add /D15
P3_6/A14	P3_6/A14(/D14)	Add /D14
P3_5/A13	P3_5/A13(/D13)	Add /D13
P3_4/A12	P3_4/A12(/D12)	Add /D12
P3_3/A11	P3_3/A11(/D11)	Add /D11
P3_2/A10	P3_2/A10(/D10)	Add /D10
P3_1/A9	P3_1/A9(/D9)	Add /D9

Table 3.2.2 Differences of Pin Characteristics (2/2)

M16C/62P	M32C/84	Differences from M16C/62P
P3_0/A8(/-/D7)	P3_0/A8(/D8)	Add /D8 Delete /-/D7
P2_7/AN2_7/A7(/D7/D6)	P2_7/AN2_7/A7(/D7)	Delete /D6
P2_6/AN2_6/A6(/D6/D5)	P2_6/AN2_6/A6(/D6)	Delete /D5
P2_5/AN2_5/A5(/D5/D4)	P2_5/AN2_5/A5(/D5)	Delete /D4
P2_4/AN2_4/A4(/D4/D3)	P2_4/AN2_4/A4(/D4)	Delete /D3
P2_3/AN2_3/A3(/D3/D2)	P2_3/AN2_3/A3(/D3)	Delete /D2
P2_2/AN2_2/A2(/D2/D1)	P2_2/AN2_2/A2(/D2)	Delete /D1
P2_1/AN2_1/A1(/D1/D0)	P2_1/AN2_1/A1(/D1)	Delete /D0
P2_0/AN2_0/A0(/D0/-)	P2_0/AN2_0/A0(/D0)	Delete /-
P11_7	-	Only M16C/62P
P11_6		
P11_5		
P11_3	P11_3/INPC1_3/OUTC1_3	Add INPC1_3/OUTC1_3
P11_2	P11_2/INPC1_2/OUTC1_2/ISRXD1/BE1IN	Add INPC1_2/OUTC1_2/ISRXD1/BE1IN
P11_1	P11_1/INPC1_1/OUTC1_1/ISCLK1	Add INPC1_1/OUTC1_1/ISCLK1
P11_0	P11_0/INPC1_0/OUTC1_0/ISTXD1/BE1OUT	Add INPC1_0/OUTC1_0/ISTXD1/BE1OUT
-	P14_6	Only M32C/84
	P14_5	
	P14_4	
	P14_3/INPC1_7/OUTC1_7	
	P14_2/INPC1_6/OUTC1_6	
	P15_7/AN15_7	
	P15_6/AN15_6	
	P15_5/AN15_5	
	P15_4/AN15_4	
	P15_3/AN15_3	
	P15_2/ISRXD0/AN15_2	
	P15_1/ISCLK0/AN15_1	
	P15_0/ISTXD0/AN15_0	

4. Detailed Differences

4.1 Differences of CPU Functions

Table 4.1.1 lists the differences of Instructions, Table 4.1.2 lists the differences of CPU registers, and Table 4.1.3 lists the differences of register banks.

Table 4.1.1 Differences of Instructions

Item	M16C/62P	M32C/84
Additional Instructions	-	ADDX, BITINDEX, BRK2, CLIP, CMPX, EXTZ, FREIT, INDEXcnd, MAX, MIN, MOVX, MULEX, SCcnd, SCMPU, SHANC, SHLNC, SIN, SMOVU, SOUT, SUBX
Deleted Instructions	-	LDE (use MOV instruction) STE (use MOV instruction) LDINTB (use LDC #IMM, INTB)
Bit Operation	Register bit 0 to 15 can be operated BSET bit, R0 (bit 0 to 15)	Register bit 0 to 7 can be operated BSET bit, R0L (bit 0 to 7) BSET bit, R0H (bit 0 to 7)

Table 4.1.2 Differences of Bit Length

Internal register		M16C/62P	M32C/84
Address register	A0, A1	16 bit	24 bit
Static base register	SB		
Frame base register	FB		
User stack pointer	USP		
Interrupt stack pointer	ISP		
Interrupt table register	INTB	20 bit	24 bit
	INTBL	16 bit	-
	INTBH	4 bit	-
Program counter	PC	20 bit	24 bit
High-speed interrupt register	SVF	-	16 bit
	SVP	-	16 bit
	VCT	-	24 bit
DMAC associated register (When using three or more DMAC channels, Register bank 1 and high-speed interrupt register are extended for use as DMAC register)	DMD0, DMD1	-	8 bit
	DCT0, DCT1, DCT2(R0), DCT3(R1)	-	16 bit
	DRC0, DRC1, DRC2(R2), DRC3(R3)	-	16 bit
	DMA0, DMA1, DMA2(A0), DMA3(A1)	-	24 bit
	DRA0, DRA1, DRA2(SVP), DRA3(VCT)	-	24 bit
	DSA0, DSA1, DSA2(SB), DSA3(FB)	-	24 bit

Table 4.1.3 Differences of Register Banks

Internal register		M16C/62P	M32C/84
Static base register	SB	Register bank 0	Register bank 0 Register bank 1

4.2 Differences of Reset

There are five kinds of reset which are hardware reset 1, low voltage detection reset (hardware reset 2), software reset, watchdog timer reset, and oscillation stop detection reset (only M16C/62P). Some of SFR maintain values set before reset, even after each reset has been performed. Table 4.2.1 lists details.

Table 4.2.1 Register Maintaining Values Even after Reset

Kind of reset	Register	Value after reset	
		M16C/62P	M32C/84
Hardware reset 1	PUR1	Varies according to CNVSS level 00h (CNVSS pin "L") 02h (CNVSS pin "H")	Initialized regardless of the CNVSS level
	WDC	WDC5 bit is not initialized	
Low voltage detection reset (Hardware reset 2)	PUR1	Varies according to CNVSS level 00h (CNVSS pin "L") 02h (CNVSS pin "H")	Initialized regardless of the CNVSS level
	WDC	WDC5 bit is not initialized	
Software reset	PM0	Bits PM01 and PM00 are not initialized	
	VCR1	Not initialized	Initialized
	VCR2	Not initialized	Initialized
	PUR1	Varies according to the value of registers PM01 and PM00 00h (PM01, PM00 = 00b) 02h (PM01, PM00 = 01b) 02h (PM01, PM00 = 11b)	Initialized regardless of the CNVSS level
	TCSPR	-	Not initialized
	WDC	WDC5 bit is not initialized	
Watchdog timer reset	PM0	Bits PM01 and PM00 are not initialized	
	VCR1	Not initialized	Initialized
	VCR2	Not initialized	Initialized
	PUR1	Varies according to the value of registers PM01 and PM00 00h (PM01, PM00 = 00b) 02h (PM01, PM00 = 01b) 02h (PM01, PM00 = 11b)	Initialized regardless of the CNVSS level
	TCSPR	-	Not initialized
	WDC	WDC5 bit is not initialized	
Oscillation stop detection reset	PM0	Bits PM01 and PM00 are not initialized	-
	CM2	Bits CM20, CM21 and CM27 are not initialized	-
	VCR1	Not initialized	-
	VCR2	Not initialized	-
	PUR1	Varies according to the value of registers PM01 and PM00 00h (PM01, PM00 = 00b) 02h (PM01, PM00 = 01b) 02h (PM01, PM00 = 11b)	-
	WDC	WDC5 bit is not initialized	-

4.3 Differences of Low Voltage Detection Circuit

Table 4.3.1 lists the differences of low voltage detection circuit associated SFR.

Table 4.3.1 Differences of Low Voltage Detection Circuit associated SFR

Symbol	Address		bit	Differences	
	M16C/62P	M32C/84		M16C/62P	M32C/84
VCR1	0019h	001Bh	-	Different address	
VCR2	001Ah	0017h	-	Different address	
D4INT	001Fh	002Fh	1	STOP Mode Deactivation Control	STOP/WAIT Mode Deactivation Control
			6-7	Nothing is assigned.	Reserved bit

4.4 Differences of Processor Mode

Table 4.4.1 lists the differences of processor mode associated SFR.

Table 4.4.1 Differences of Processor Mode associated SFR

Symbol	Address		bit	Differences	
	M16C/62P	M32C/84		M16C/62P	M32C/84
PM0	0004h	0004h	6	Ports P4_0 to P4_3 Function Select	Reserved bit
			7	BCLK Output Disable	BCLK Output Disable
PM1	0005h	0005h	0	CS2 Area Switch	External Memory Space Mode
			1	Ports P3_7 to P3_4 Function Select	
			2	Watchdog Timer Function Select	Internal Memory Wait
			3	Internal Reserved Area Expansion	SFR Area Wait
			4-5	Memory Area Expansion	ALE Pin Select
			7	Wait Bit	Reserved bit

4.5 Differences of Bus

Table 4.5.1 lists the Differences of bus, Table 4.5.2 lists the Differences of bus setting, Table 4.5.3 lists the Differences of bus control pin, and Table 4.5.4 lists the Differences of bus associated SFR.

Table 4.5.1 Differences of Bus

Item	M16C/62P	M32C/84
Address space	1-Mbyte / 4-Mbyte (refer to memory space expansion function)	16-Mbyte
Address bus width	12 bit / 16bit / 20bit	24 bit fixed
External Area wait	1 to 3 waits	1 to 7 waits
Recovery Cycle Addition	N/A	Available
Page Mode	N/A	Available (Only ROMless version)
SFR Area wait number	1 wait / 2 waits (at PLL operation)	1 wait / 2 waits

Table 4.5.2 Differences of Bus Setting

Item	M16C/62P	M32C/84
Address bus width	PM06 bit in the PM0 register PM11 bit in the PM1 register	-
Data bus width	Set bus width in all area BYTE pin "H" : 8 bit bus width "L" : 16 bit bus width	Set bus width per external space Bits DS0 to DS3 in the DS register 0 : 8 bit bus width 1 : 16 bit bus width Set bus width after reset Only the external space 3 is set by BYTE pin. BYTE pin "H" : 8 bit bus width "L" : 16 bit bus width
Chip select signal	Csi bit (i = 0 to 3) in the CSR register	Bits PM10 and PM11 in the PM1 register
SFR Area wait number	PM20 bit in the PM2 register	PM13 bit in the PM1 register
External Area wait	CsiW bit in the CSR register Bits CSEi0 and CSEi1 in the CSE register	Bits EWCRi00 to EWCRi04 in the EWCRi register (i = 0 to 3)
Recovery Cycle Addition	-	EWCRi06 bit in the EWCRi register
BCLK output	PM07 bit in the PM0 register	PM07 bit in the PM0 register Bits CM00 and CM01 in the CM0 register

Table 4.5.3 Differences of Bus associated Pin

Pin name	M16C/62P	M32C/84
ALE	P5_6	P5_6
		P5_4/$\overline{\text{HLDA}}$
		P5_3/CLKOUT/BCLK
$\overline{\text{CS0}}$	P4_4	P4_7/$\overline{\text{A23}}$
$\overline{\text{CS1}}$	P4_5	P4_6/A22
$\overline{\text{CS2}}$	P4_6	P4_5/A21
$\overline{\text{CS3}}$	P4_7	P4_4/A20
Multiplexed bus associated	P3_7/A15	P3_7/A15(/D15)
	P3_6/A14	P3_6/A14(/D14)
	P3_5/A13	P3_5/A13(/D13)
	P3_4/A12	P3_4/A12(/D12)
	P3_3/A11	P3_3/A11(/D11)
	P3_2/A10	P3_2/A10(/D10)
	P3_1/A9	P3_1/A9(/D9)
	P3_0/A8(/-/D7)	P3_0/A8(/D8)
	P2_7/A7(/D7/D6)	P2_7/A7(/D7)
	P2_6/A6(/D6/D5)	P2_6/A6(/D6)
	P2_5/A5(/D5/D4)	P2_5/A5(/D5)
	P2_4/A4(/D4/D3)	P2_4/A4(/D4)
	P2_3/A3(/D3/D2)	P2_3/A3(/D3)
	P2_2/A2(/D2/D1)	P2_2/A2(/D2)
	P2_1/A1(/D1/D0)	P2_1/A1(/D1)
	P2_0/A0(/D0/-)	P2_0/A0(/D0)

Table 4.5.4 Differences of Bus associated SFR

Symbol	Address		bit	Differences	
	M16C/62P	M32C/84		M16C/62P	M32C/84
CSR	0008h	-	-	Only M16C/62P	-
CSE	001Bh	-	-	Only M16C/62P	-
DBR	000Bh	-	-	Only M16C/62P	-
DS	-	000Bh	-	-	Only M32C/84
EWCR0	-	0048h	-	-	Only M32C/84
EWCR1	-	0049h	-	-	Only M32C/84
EWCR2	-	004Ah	-	-	Only M32C/84
EWCR3	-	004Bh	-	-	Only M32C/84
PWCR0	-	004Ch	-	-	Only M32C/84
PWCR1	-	004Dh	-	-	Only M32C/84

4.6 Differences of Clock

Table 4.6.1 lists the Differences of clock, Table 4.6.2 lists the Differences of clock associated setting, Table 4.6.3 lists the Differences of clock associated pin, and Table 4.6.4 lists the Differences of clock associated SFR.

Table 4.6.1 Differences of Clock

Item	M16C/62P	M32C/84
XIN-XOUT Drive Capacity	Enable to switch	Unable to switch
Main Clock Division	Select from no division, 2, 4, 8, 16 division	Select from no division, 2, 3, 4, 6, 8, 10, 12, 14, 16 division
Peripheral Function Clock	f1, f2(1), f8, f32, f1SIO, f2SIO, f8SIO, f32SIO fAD, fc32	f1, f8, f32(2), f2n(3) fAD, fc32, fCAN
PLL Multiplying Factor	Multiply-by-2/ Multiply-by-4/ Multiply-by-6/ Multiply-by-8	Divide-by-2 or Divide-by-3 after Multiply-by-6, Multiply-by-8
Operations when Oscillation Stop	Oscillation Stop Detection Reset/ Oscillation Stop, Re-oscillation Stop Interrupt	Oscillation Stop Detection Interrupt
Oscillation Stop Detect Function	Detect Oscillation Stop, Re-oscillation	Detect Oscillation Stop
Wait mode, Stop mode	Exiting procedure is different between M16C/62P and M32C/84.	
Transition from low-speed mode or low-power mode to stop mode	Enable	Disable
Transition from on-chip oscillator mode to stop mode		

The underlined items represent the differences between the two MCUs.

NOTES:

1. f1 or f2 is selected as a count source of the timers A and B and as an operating clock of the serial I/O by setting PCLKR register.
2. f32 is not selected as a count source of the timers but is selected for the CLKOUT pin output.
3. f2 is not used in M32C/84 and f2n is used as the clock (n = 0 to 15, (n = 0 : no division)).

Table 4.6.2 Differences of Clock associated Setting

Item	M16C/62P	M32C/84
XIN-XOUT Drive Capacity	CM15 bit in the CM1 register	-
Main Clock Division	CM06 bit in the CM0 register Bits CM16 and CM17 in the CM1 register	Bits MCD0 to MCD4 in MCD register
PLL Multiplying Factor	PLC0 register	PLC0 register PLC1 register
Operation Select (when an oscillation stop)	CM27 bit in the CM2 register	-

Table 4.6.3 Differences of Clock associated Pin

Pin name	M16C/62P	M32C/84
CLKOUT	P5_7	P5_3

Table 4.6.4 Differences of Clock associated SFR

Symbol	Address		bit	Differences	
	M16C/62P	M32C/84		M16C/62P	M32C/84
CM0	0006h	0006h	6	Main Clock Division Select 0	Watchdog Timer Function Select
CM1	0007h	0007h	1	System Clock Select 1	Reserved bit
			5	XIN-XOUT Drive Capacity Select Bit	Reserved bit
			6	Main Clock Division Select	Reserved bit
			7		CPU Clock Select Bit 1
CM2	000Ch	000Dh	0	Oscillation Stop, Re-Oscillation Detection Enable	Oscillation Stop Detection Enable
			1	System Clock Select 2	CPU Clock Select Bit 2
			2	Oscillation Stop, Re-Oscillation Detection Flag	Oscillation Stop Detection Flag
			6	Nothing is assigned.	Reserved bit
			7	Operation Select (when an oscillation stop, re-oscillation is detected)	Reserved bit
MCD	-	000Ch	-	-	Only M32C/84
PCLKR	025Eh	-	-	Only M16C/62P	-
PLC0	001Ch	0026h	0-2	PLL Multiplying Factor Select (Multiply-by-2, 4, 6, 8)	PLL Multiplying Factor Select (Multiply-by-6, 8)
PLC1	-	0027h	-	-	Only M32C/84
PM2	001Eh	0013h	0	Specifying Wait when Accessing SFR at PLL Operation	Reserved bit
			4	Reserved bit	CPU Clock Select 3
			5	Nothing is assigned.	CAN Clock Select
			6-7	Nothing is assigned.	f2n Count source Select
TCSPR	-	035Fh	-	-	Only M32C/84

4.7 Differences of Protection

Table 4.7.1 lists the differences of protection associated SFR.

Table 4.7.1 Differences of Protection associated SFR

Symbol	Address		bit	Differences	
	M16C/62P	M32C/84		M16C/62P	M32C/84
PRCR	000Ah	000Ah	0	Protect 0 Enables writing to registers CM0, CM1, CM2, PLC0, and PCLKR	Protect 0 Enables writing to registers CM0, CM1, CM2, MCD, PLC0, and PLC1
			1	Protect 1 Enables writing to registers PM0, PM1, PM2, TB2SC, INVC0, and INVC1	Protect 1 Enables writing to registers PM0, PM1, PM2, INVC0, and INVC1
			2	Protect 2 Enables writing to registers PD9, S3C, and S4C	Protect 2 Enables writing to registers PD9 and PS3

The underlined items represent the differences between the two MCUs.

4.8 Differences of Interrupt

Table 4.8.1 lists the differences of interrupt and Tables 4.8.2 and 4.8.3 list the differences of interrupt associated SFR. The re-locatable vector tables and the interrupt priority level select circuits are different.

Table 4.8.1 Differences of Interrupt

Item	M16C/62P	M32C/84
High-speed interrupt	N/A	Available
Address match interrupt	Can be set in 4 addresses	Can be set in 8 addresses

Table 4.8.2 Differences of Interrupt associated SFR (1/2)

Symbol	Address		bit	Differences	
	M16C/62P	M32C/84		M16C/62P	M32C/84
AD0IC	-	0073h	-	-	Only M32C/84
ADIC	004Eh	-	-	Only M16C/62P	-
AIER	0009h	0009h	2	Nothing is assigned.	Enables Address Match Interrupt 2
			3	Nothing is assigned.	Enables Address Match Interrupt 3
			4	Nothing is assigned.	Enables Address Match Interrupt 4
			5	Nothing is assigned.	Enables Address Match Interrupt 5
			6	Nothing is assigned.	Enables Address Match Interrupt 6
			7	Nothing is assigned.	Enables Address Match Interrupt 7
AIER2	01BBh	-	-	Only M16C/62P	-
BCN0IC/ BCN3IC	-	0071h	-	-	Only M32C/84
BCN1IC/ BCN4IC	-	0091h	-	-	Only M32C/84
BCN2IC	-	008Fh	-	-	Only M32C/84
BCNIC	004Ah	-	-	Only M16C/62P	-
DM0IC	004Bh	0068h	-	Different address	
DM1IC	004Ch	0088h	-	Different address	
DM2IC	-	006Ah	-	-	Only M32C/84
DM3IC	-	008Ah	-	-	Only M32C/84

Table 4.8.3 Differences of Interrupt associated SFR (1/2)

Symbol	Address		bit	Differences	
	M16C/62P	M32C/84		M16C/62P	M32C/84
IFSR	035Fh	031Fh	6	Interrupt Source Select (SI/O3 / $\overline{INT4}$)	Interrupt Source Select (UART0 / UART3)
			7	Interrupt Source Select (SI/O4 / $\overline{INT5}$)	Interrupt Source Select (UART1 / UART4)
IFSR2A	035Eh	-	-	Only M16C/62P	-
INT0IC	005Dh	009Eh	5	Reserved bit	Level / Edge Sensitive Switch Bit
INT1IC	005Eh	007Eh	5	Reserved bit	Level / Edge Sensitive Switch Bit
INT2IC	005Fh	009Ch	5	Reserved bit	Level / Edge Sensitive Switch Bit
INT3IC	0044h	007Ch	5	Reserved bit	Level / Edge Sensitive Switch Bit
INT4IC	0049h	009Ah	5	Reserved bit	Level / Edge Sensitive Switch Bit
INT5IC	0048h	007Ah	5	Reserved bit	Level / Edge Sensitive Switch Bit
KUPIC	004Dh	0093h	-	Different address	
RLVL	-	009Fh	-	-	Only M32C/84
RMAD0	0010h-0012h	0010h-0012h	-	Setting Range : 20 bit	Setting Range : 24 bit
RMAD1	0014h-0016h	0014h-0016h	-	Setting Range : 20 bit	Setting Range : 24 bit
RMAD2	01B8h-01BAh	0018h-001Ah	-	Setting Range : 20 bit	Setting Range : 24 bit
RMAD3	01BCh-01BEh	001Ch-001Eh	-	Setting Range : 20 bit	Setting Range : 24 bit
RMAD4	-	0028h-002Ah	-	-	Only M32C/84, Setting Range : 24 bit
RMAD5	-	002Ch-002Eh	-	-	Only M32C/84, Setting Range : 24 bit
RMAD6	-	0038h-003Ah	-	-	Only M32C/84, Setting Range : 24 bit
RMAD7	-	003Ch-003Eh	-	-	Only M32C/84, Setting Range : 24 bit
S0RIC	0052h	0072h	-	Different address	
S0TIC	0051h	0090h	-	Different address	
S1RIC	0054h	0074h	-	Different address	
S1TIC	0053h	0092h	-	Different address	
S2RIC	0050h	006Bh	-	Different address	
S2TIC	004Fh	0089h	-	Different address	
S3IC	0049h	-	-	Only M16C/62P	-
S3RIC	-	006Dh	-	-	Only M32C/84
S3TIC	-	008Bh	-	-	Only M32C/84
S4RIC	-	006Fh	-	-	Only M32C/84
S4TIC	-	008Dh	-	-	Only M32C/84
S4IC	0048h	-	-	Only M16C/62P	-
TA0IC	0055h	006Ch	-	Different address	
TA1IC	0056h	008Ch	-	Different address	
TA2IC	0057h	006Eh	-	Different address	
TA3IC	0058h	008Eh	-	Different address	
TA4IC	0059h	0070h	-	Different address	
TB0IC	005Ah	0094h	-	Different address	
TB1IC	005Bh	0076h	-	Different address	
TB2IC	005Ch	0096h	-	Different address	
TB3IC	0047h	0078h	-	Different address	
TB4IC	0046h	0098h	-	Different address	
TB5IC	0045h	0069h	-	Different address	

4.9 Differences of Watchdog Timer

Table 4.9.1 lists the differences of Watchdog Timer.

Table 4.9.1 Differences of Watchdog Timer

Item	M16C/62P	M32C/84
Watchdog Timer Function Select (selects interrupt or reset)	PM12 bit in the PM1 register	CM06 bit in the CM0 register

4.10 Differences of DMAC

Table 4.10.1 lists the Differences of DMAC, Table 4.10.2 lists the differences of DMAC settings, and Table 4.10.3 lists the differences of DMAC associated SFR. DMAC associated registers are assigned to SFR in M16C/62P and are assigned to internal register and SFR in M32C/84. Therefore, DMAC settings procedures are different between M16C/62P and M32C/84.

Table 4.10.1 Differences of DMAC

Item	M16C/62P	M32C/84
DMAC-Associated register	Assigned to SFR	Assigned to internal register and SFR
Number of Channels	2 channels	4 channels
Transfer Memory Space	- From a given address in a 1-Mbyte space to a fixed address - From a fixed address to a given address in a 1-Mbyte space - From a fixed address to a fixed address	- From a given address in a 16-Mbyte space to a fixed address - From a fixed address to a given address in a 16-Mbyte space
Number of Transfer Time	Number set in DMAi transfer counter (i = 0 to 1) +1	Number set in DMAi transfer counter (i = 0 to 3)
Interrupt Request Generation Timing	When the DMAi transfer counter underflows	When the DMAi transfer counter changes ”0001h” to ”0000h”

Table 4.10.2 Differences of DMAC Settings

Item	M16C/62P	M32C/84
DMA Transfer Factor Select	Set bits DSEL0 to DSEL3 and DMS bit in the DMiSL register	Set DSEL0 to DSEL4 bit in the DMiSL register
Transfer Mode	DMiCON register	Set DMDi register
Source Address	SARi register	When the Source Address is fixed: DSAi register When the Source Address is in memory: DMAi register (Re-loaded value in repeat transfer mode is set to DRAi register)
Destination Address	DARi register	
Transfer Count	Set (the number of transfers - 1) to TCRi register.	Set the number of transfers to DCTi register (Re-loaded value in repeat transfer mode is set to DRCi register)

Table 4.10.3 Differences of DMAC associated SFR

Symbol	Address		bit	Differences	
	M16C/62P	M32C/84		M16C/62P	M32C/84
DAR0	0024h-0026h	-	-	Only M16C/62P	-
DAR1	0034h-0036h	-	-	Only M16C/62P	-
DCT0 to DCT3	-	CPU internal register	-	-	Only M32C/84 DCT0(1), DCT1(1) DCT2(2), DCT3(2)
DM0CON	002Ch	-	-	Only M16C/62P	-
DM0SL	03B8h	0378h	0-3	DMA Request Factor Select	DMA Request Factor Select
			4	Nothing is assigned.	
			5	Nothing is assigned.	Software DMA Request
			6	DMA Request Factor Expansion Select	Reserved bit
			7	Software DMA Request	DMA Request
DM1CON	003Ch	-	-	Only M16C/62P	-
DM1SL	03BAh	0379h	0-3	DMA Request Factor Select	DMA Request Factor Select
			4	Nothing is assigned.	
			5	Nothing is assigned.	Software DMA Request
			6	DMA Request Factor Expansion Select	Reserved bit
			7	Software DMA Request	DMA Request
DM2SL	-	037Ah	-	-	Only M32C/84
DM3SL	-	037Bh	-	-	Only M32C/84
DMA0 to DMA3	-	CPU internal register	-	-	Only M32C/84 DMA0(1), DMA1(1) DMA2(2), DMA3(2)
DMD0 DMD1	-	CPU internal register	-	-	Only M32C/84(1)
DRA0 to DRA3	-	CPU internal register	-	-	Only M32C/84 DRA0(1), DRA1(1) DRA2(1)(2), DRA3(1)(2)
DRC0 to DRC3	-	CPU internal register	-	-	Only M32C/84 DRC0(1), DRC1(1) DRC2(2), DRC3(2)
DSA0 to DSA3	-	CPU internal register	-	-	Only M32C/84 DSA0(1), DSA1(1) DSA2(1)(2), DSA3(1)(2)
SAR0	0020h-0022h	-	-	Only M16C/62P	-
SAR1	0030h-0032h	-	-	Only M16C/62P	-
TCR0	0028h-0029h	-	-	Only M16C/62P	-
TCR1	0038h-0039h	-	-	Only M16C/62P	-

NOTES:

1. Use the LDC instruction to set the registers.
2. Use the register bank 1 or the high-speed interrupt registers when DMA2 and/or DMA3 is used.

4.11 Differences of Timer

Table 4.11.1 lists the differences of timer and Table 4.11.2 lists the differences of timer associated SFR.

Table 4.11.1 Differences of Timer

Item	M16C/62P	M32C/84
Count Source	f1/f2, f8, f32, fc32	f1, f8, f2n, fc32
Pulse output function select	MR0 bit (i = 0 to 4) in the TAiMR register	Function select register

The underlined items represent the differences between the two MCUs.

Table 4.11.1 Differences of Timer associated SFR

Symbol	Address		bit	Differences	
	M16C/62P	M32C/84		M16C/62P	M32C/84
ONSF	0382h	0342h	-	Different address	
TA0 to TA4	0386h-0387h to 038Eh-038Fh	0346h-0347h to 034Eh-034Fh	-	Different address	
TA0MR	0396h	0356h	2	Pulse output function select	Reserved bit
			6-7	Count Source select (f1/f2, f32)	Count Source select (f1, f2n)
TA1MR	0397h	0357h	2	Pulse output function select	Reserved bit
			6-7	Count Source select (f1/f2, f32)	Count Source select (f1, f2n)
TA2MR	0398h	0358h	2	Pulse output function select	Reserved bit
			6-7	Count Source select (f1/f2, f32)	Count Source select (f1, f2n)
TA3MR	0399h	0359h	2	Pulse output function select	Reserved bit
			6-7	Count Source select (f1/f2, f32)	Count Source select (f1, f2n)
TA4MR	039Ah	035Ah	2	Pulse output function select	Reserved bit
			6-7	Count Source select (f1/f2, f32)	Count Source select (f1, f2n)
TABSR	0380h	0340h	-	Different address	
TB0 to TB2	0390h-0391h to 0394h-0395h	0350h-0351h to 0354h-0355h	-	Different address	
TB0MR	039Bh	035Bh	6-7	Count Source select (f1/f2,f32)	Count Source select (f1,f2n)
TB1MR	039Ch	035Ch	6-7	Count Source select (f1/f2,f32)	Count Source select (f1,f2n)
TB2MR	039Dh	035Dh	6-7	Count Source select (f1/f2,f32)	Count Source select (f1,f2n)
TB3 to TB5	0350h-0351h to 0354h-0355h	0310h-0311h to 0314h-0315h	-	Different address	
TB3MR	035Bh	031Bh	6-7	Count Source select (f1/f2,f32)	Count Source select (f1,f2n)
TB4MR	035Ch	031Ch	6-7	Count Source select (f1/f2,f32)	Count Source select (f1,f2n)
TB5MR	035Dh	031Dh	6-7	Count Source select (f1/f2,f32)	Count Source select (f1,f2n)
TBSR	0340h	0300h	-	Different address	
TRGSR	0383h	0343h	-	Different address	
UDF	0384h	0344h	-	Different address	
TCSPR	-	035Fh	-		Only M32C/84

4.12 Three-Phase Motor Control Timer Functions

Table 4.12.1 lists the differences of three-phase motor control timer functions associated SFR.

Table 4.12.1 Differences of Three-Phase Motor Control Timer Functions associated SFR

Symbol	Address		bit	Differences	
	M16C/62P	M32C/84		M16C/62P	M32C/84
DTT	034Ch	030Ch	-	Different address	
ICTB2	034Dh	030Dh	-	Different address	
IDB0	034Ah	030Ah	-	Different address	
IDB1	034Bh	030Bh	-	Different address	
INVC0	0348h	0308h	-	Different address	
INVC1	0349h	0309h	2	Dead Time Timer Count Source (f1/f2 or f1 divided-by-2 / f2 divided-by-2)	Dead Time Timer Count Source (f1 / f1 divided-by-2)
TA11	0342h-0343h	0302h-0303h	-	Different address	
TA21	0344h-0345h	0304h-0305h	-	Different address	
TA41	0346h-0347h	0306h-0307h	-	Different address	
TB2SC	039Eh	035Eh	1	Three Phase Output Port $\overline{NMI}$ Control	Reserved bit (Set to 0.)

4.13 Differences of Serial Interface

Table 4.13.1 lists the differences of serial interface, Table 4.13.2 lists the differences of serial interface associated pin, and Tables 4.13.3 and 4.13.4 list the differences of serial interface associated SFR. To output from each serial interface associated pin in M32C/84, set using the function select registers.

Table 4.13.1 Differences of Serial Interface

Item	M16C/62P	M32C/84
Configuration	3 channels (UART0 to UART2) Clock Synchronous Clock Asynchronous I^2C Mode Special Mode2 IE Mode SIM Mode 2 channels (SI/O3, SI/O4) Clock Synchronous	5 channels (UART0 to UART4) Clock Synchronous Clock Asynchronous I^2C Mode Special Mode 2 GCI Mode IE Mode SIM Mode
Count Source	f1/f2, f8, f32	f1, f8, f2n
Transfer Clock Output from multiple pins Function	Selectable using UART1	N/A
$\overline{CTS}/\overline{RTS}$ Separate Function	Selectable using UART0	N/A
Pin Output Settings	When using UART associated registers	When using Function Select Registers

The underlined items represent the differences between the two MCUs.

Table 4.13.2 Differences of Serial Interface associated Pin

Channel	Pin	M16C/62P	M32C/84
UART0	P6_0	$\overline{CTS0}$/$\overline{RTS0}$	$\overline{CTS0}$/$\overline{RTS0}$/$\overline{SS0}$
	P6_1	CLK0	CLK0
	P6_2	RXD0/SCL0	RXD0/SCL0/STXD0
	P6_3	TXD0/SDA0	TXD0/SDA0/SRXD0
UART1	P6_4	$\overline{CTS1}$/$\overline{RTS1}$/$\overline{CTS0}$/CLKS1	$\overline{CTS1}$/$\overline{RTS1}$/$\overline{SS1}$
	P6_5	CLK1	CLK1
	P6_6	RXD1/SCL1	RXD1/SCL1/STXD1
	P6_7	TXD1/SDA1	TXD1/SDA1/SRXD1
UART2	P7_0	TXD2/SDA2	TXD2/SDA2/SRXD2
	P7_1	RXD2/SCL2	RXD2/SCL2/STXD2
	P7_2	CLK2	CLK2
	P7_3	$\overline{CTS2}$/$\overline{RTS2}$	$\overline{CTS2}$/$\overline{RTS2}$/$\overline{SS2}$
UART3 / SI/O3	P9_0	CLK3	CLK3
	P9_1	SIN3	RXD3/SCL3/STXD3
	P9_2	SOUT3	TXD3/SDA3/SRXD3
	P9_3	-	$\overline{CTS3}$/$\overline{RTS3}$/$\overline{SS3}$
UART4 / SI/O4	P9_4	-	$\overline{CTS4}$/$\overline{RTS4}$/$\overline{SS4}$
	P9_5	CLK4	CLK4
	P9_6	SOUT4	TXD4/SDA4/SRXD4
	P9_7	SIN4	RXD4/SCL4/STXD4

Table 4.13.3 Differences of Serial Interface associated SFR (1/2)

Symbol	Address		bit	Differences	
	M16C/62P	M32C/84		M16C/62P	M32C/84
U0BRG	03A1h	0369h	-	Different address	
U0C0	03A4h	036Ch	0-1	UiBRG Count Source Select (f1/f2, f32)	UiBRG Count Source Select (f1, f2n)
U0C1	03A5h	036Dh	4	Nothing is assigned.	UARTi Transmit Interrupt Cause Select
			5	Nothing is assigned.	UARTi Continuous Receive Mode Enable
			7	Error Signal Output Enable	Clock-Divided Synchronous Stop/ Error Signal Output Enable
U0MR	03A0h	0368h	-	Different address	
U0RB	03A6h-03A7h	036Eh-036Fh	-	Different address	
U0SMR	036Fh	0367h	3	Reserved bit	SCLL Sync Output Enable
			7	Nothing is assigned.	Clock Divide Synchronous
U0SMR2	036Eh	0366h	7	Nothing is assigned.	External Clock Synchronous Enable
U0SMR3	036Dh	0365h	0	Nothing is assigned.	$\overline{SS}$ Pin Function Enable
			2	Nothing is assigned.	Serial Input Port Set
			4	Nothing is assigned.	Fault Error Flag
U0SMR4	036Ch	0364h	3	SCL, SDA Output Select (Start and Stop Condition output/ not output)	SCL, SDA Output Select (Selects the serial I/O / Selects the start/stop condition)
U0TB	03A2h-03A3h	036Ah-036Bh	-	Different address	
U1BRG	03A9h	02E9h	-	Different address	
U1C0	03ACh	02ECh	0-1	UiBRG Count Source Select (f1/f2, f32)	UiBRG Count Source Select (f1, f2n)
U1C1	03ADh	02EDh	4	Nothing is assigned.	UARTi Transmit Interrupt Cause Select
			5	Nothing is assigned.	UARTi Continuous Receive Mode Enable
			7	Error Signal Output Enable	Clock-Divided Synchronous Stop/ Error Signal Output Enable
U1MR	03A8h	02E8h	-	Different address	
U1RB	03AEh-03AFh	02EEh-02EFh	-	Different address	
U1SMR	0373h	02E7h	3	Reserved bit	SCLL Sync Output Enable
			7	Nothing is assigned.	Clock Divide Synchronous
U1SMR2	0372h	02E6h	7	Nothing is assigned.	External Clock Synchronous Enable
U1SMR3	0371h	02E5h	0	Nothing is assigned.	$\overline{SS}$ Pin Function Enable
			2	Nothing is assigned.	Serial Input Port Set
			4	Nothing is assigned.	Fault Error Flag
U1SMR4	0370h	02E4h	3	SCL, SDA Output Select (Start and Stop Condition output/ not output)	SCL, SDA Output Select (Selects the serial I/O / Selects the start/stop condition)
U1TB	03AAh-03ABh	02EAh-02EBh	-	Different address	
U2BRG	0379h	0339h	-	Different address	
U2C0	037Ch	033Ch	0-1	UiBRG Count Source Select (f1/f2, f32)	UiBRG Count Source Select (f1, f2n)
U2C1	037Dh	033Dh	7	Error Signal Output Enable	Clock-Divided Synchronous Stop/ Error Signal Output Enable
U2MR	0378h	0338h	-	Different address	
U2RB	037Eh-037Fh	033Eh-033Fh	-	Different address	
U2SMR	0377h	0337h	3	Reserved bit	SCLL Sync Output Enable
			7	Nothing is assigned.	Clock Divide Synchronous
U2SMR2	0376h	0336h	7	Nothing is assigned.	External Clock Synchronous Enable

Table 4.13.4 Differences of Serial Interface associated SFR (2/2)

Symbol	Address		bit	Differences	
	M16C/62P	M32C/84		M16C/62P	M32C/84
U2SMR3	0375h	0335h	0	Nothing is assigned.	$\overline{SS}$ Pin Function Enable
			2	Nothing is assigned.	Serial Input Port Set
			4	Nothing is assigned.	Fault Error Flag
U2SMR4	0374h	0334h	3	SCL, SDA Output Select (Start and Stop Condition output/ not output)	SCL, SDA Output Select (Selects the serial I/O / Selects the start/stop condition)
U2TB	037Ah-03ABh	033Ah-033Bh	-	Different address	
UCON	03B0h	-	-	Only M16C/62P	-
S3BRG	0363h	-	-	Only M16C/62P	-
S3C	0362h	-	-	Only M16C/62P	-
S3TRR	0360h	-	-	Only M16C/62P	-
S4BRG	0367h	-	-	Only M16C/62P	-
S4C	0366h	-	-	Only M16C/62P	-
S4TRR	0364h	-	-	Only M16C/62P	-
U3BRG	-	0329h	-	-	Only M32C/84
U3C0	-	032Ch	-	-	Only M32C/84
U3C1	-	032Dh	-	-	Only M32C/84
U3MR	-	0328h	-	-	Only M32C/84
U3RB	-	032Eh-032Fh	-	-	Only M32C/84
U3SMR	-	0327h	-	-	Only M32C/84
U3SMR2	-	0326h	-	-	Only M32C/84
U3SMR3	-	0325h	-	-	Only M32C/84
U3SMR4	-	0324h	-	-	Only M32C/84
U3TB	-	032Ah-032Bh	-	-	Only M32C/84
U4BRG	-	02F9h	-	-	Only M32C/84
U4C0	-	02FCh	-	-	Only M32C/84
U4C1	-	02FDh	-	-	Only M32C/84
U4MR	-	02F8h	-	-	Only M32C/84
U4RB	-	02FEh-02FFh	-	-	Only M32C/84
U4SMR	-	02F7h	-	-	Only M32C/84
U4SMR2	-	02F6h	-	-	Only M32C/84
U4SMR3	-	02F5h	-	-	Only M32C/84
U4SMR4	-	02F4h	-	-	Only M32C/84
U4TB	-	02FAh-02FBh	-	-	Only M32C/84

4.14 Differences of A/D Converter

4.14.1 Differences of A/D Converter

Table 4.14.1 lists the differences of A/D converter and Table 4.14.2 lists the differences of A/D converter associated SFR.

Table 4.14.1 Differences of A/D Converter

Item	M16C/62P	M32C/84
Operating Clock (ϕAD)	Selectable from among: fAD, fAD/2, fAD/3, fAD/4, fAD/6, fAD/12 (Registers ADCON0, ADCON1, and ADCON2 determine)	Selectable from among: fAD, fAD/2, fAD/3, fAD/4, fAD/6, fAD/8 (Registers AD0CON0, AD0CON1, and AD0CON3 determine)
A/D Converter maximum operating clock	VCC1 ≥ 4V : ϕAD = 12MHz VCC1 < 4V : ϕAD = 10MHz	VCC1 = 5.0 V : ϕAD = 16MHz VCC1 = 3.3 V : ϕAD = 10MHz
A/D Conversion Start Condition	Software trigger/ External trigger	Software trigger/ External trigger /Hardware trigger
Mode	One-shot mode Repeat mode Single sweep mode Repeat sweep mode 0 Repeat sweep mode 1	One-shot mode Repeat mode Single sweep mode Repeat sweep mode 0 Repeat sweep mode 1 Multi-port single sweep mode Multi-port repeat sweep mode 0
Analog Input Pins	26 pins AN0 to AN7, AN0_0 to AN0_7, AN2_0 to AN2_7, ANEX0, ANEX1	34 pins AN0 to AN7, AN0_0 to AN0_7, AN2_0 to AN2_7, AN15_0 to AN15_7, ANEX0, ANEX1
DMAC operating mode(1)	N/A	Available

NOTE:
(1) The A/D conversion result is stored in the AD00 register after the A/D conversion is completed. DMAC transfers the conversion result to a given memory space every time a pin is converted.

Table 4.14.2 Differences of A/D Converter associated SFR

Symbol	Address		bit	Differences	
	M16C/62P	M32C/84		M16C/62P	M32C/84
AD0CON0 / ADCON0	03D6h	0396h	0-2	Analog Input Pin	Analog Input Pin
			5	Trigger Select	Trigger Select
			7	Frequency Select	Frequency Select
AD0CON1 / ADCON1	03D7h	0397h	0-1	A/D Sweep Pin Select	A/D Sweep Pin Select
			4	Frequency Select 1	Frequency Select
AD0CON2 / ADCON2	03D4h	0394h	1-2	A/D Input Group Select	Analog Input Port Select
			3	Reserved bit	Nothing is assigned.
			4	Frequency Select 2	Nothing is assigned.
			5	Nothing is assigned.	External Trigger Request Cause Select
			6-7	Nothing is assigned.	Reserved bit
AD0CON3	-	0395h	-	-	Only M32C/84
AD0CON4	-	0392h	-	-	Only M32C/84
AD00 to AD07 / AD0 to AD7	03C0h-03C1h to 03CEh-03CFh	0380h-0381h to 038Eh-038Fh	-	Different address	

4.14.2 Notice of A/D Converter

In M32C/84, to separate A/D input/output pins (ANEX0, ANEX1, AN4 to AN7, and AN15_0 to AN15_7) from the other peripheral function inputs, set bits PSL3_5 and PSL3_6 in the PSL3 register, the PSC_7 bit in the PSC register and the IPS2 bit in the IPS register. Setting 1 (A/D input/output) to corresponding bits with pins which are used as A/D input/output prevents applying intermediate electric potential to the other peripheral function inputs. (Applying intermediate electric potential may bring increase of power supply current.)

4.15 Differences of D/A Converter

4.15.1 Differences of D/A Converter

Table 4.15.1 lists the Differences of D/A converter associated SFR.

Table 4.15.1 Differences of D/A Converter associated SFR

Symbol	Address		bit	Differences	
	M16C/62P	M32C/84		M16C/62P	M32C/84
DACON	03DCh	039Ch	-	Different address	
DA0	03D8h	0398h	-	Different address	
DA1	03DAh	039Ah	-	Different address	

4.15.2 Notice of D/A Converter

In M32C/84, to separate D/A output pins (DA0, DA1) from the other peripheral function inputs, set bits PSL3_3 and PSL3_4 in the PSL3 register. Setting 1 (D/A output) to corresponding bits with pins which are used as D/A output prevents applying intermediate electric potential to the other peripheral function inputs. (Applying intermediate electric potential may bring increase of power supply current.)

4.16 Differences of CRC Calculation

Table 4.16.1 lists the Differences of CRC calculation associated SFR.

Table 4.16.1 Differences of CRC Calculation associated SFR

Symbol	Address		bit	Differences	
	M16C/62P	M32C/84		M16C/62P	M32C/84
CRCIN	03BEh	037Eh	-	Different address	
CRCD	03BCh-03BDh	037Ch-037Dh	-	Different address	

4.17 Differences of Ports

4.17.1 Differences of Port Pi Direction Register, Port Pi Register

Table 4.17.1 lists the differences of port Pi direction register and port Pi register.

Table 4.17.1 Differences of Port Pi Direction Register, Port Pi Register

Symbol	Address		bit	Differences	
	M16C/62P	M32C/84		M16C/62P	M32C/84
P6	03ECh	03C0h	-	Different address	
P7	03EDh	03C1h	-	Different address	
P8	03F0h	03C4h	-	Different address	
P9	03F1h	03C5h	-	Different address	
P10	03F4h	03C8h	-	Different address	
P11	03F5h	03C9h	-	Different address	
P12	03F8h	03CCh	-	Different address	
P13	03F9h	03CDh	-	Different address	
P14	-	03D0h	-	-	Only M32C/84
P15	-	03D1h	-	-	Only M32C/84
PC14	03DEh	-	-	Only M16C/62P	-
PD6	03EEh	03C2h	-	Different address	
PD7	03EFh	03C3h	-	Different address	
PD8	03F2h	03C6h	-	Different address	
PD9	03F3h	03C7h	-	Different address	
PD10	03F6h	03CAh	-	Different address	
PD11	03F7h	03CBh	-	Different address	
PD12	03FAh	03CEh	-	Different address	
PD13	03FBh	03CFh	-	Different address	
PD14	-	03D2h	-	-	Only M32C/84
PD15	-	03D3h	-	-	Only M32C/84

4.17.2 Differences of Port Control Register

Table 4.17.2 lists the differences of port control register.

Table 4.17.2 Differences of Port Control Register

Symbol	Address		bit	Differences	
	M16C/62P	M32C/84		M16C/62P	M32C/84
PCR	03FFh	03FFh	0	Port P1 Control (Determines either the input level is read or the port latch is read)	Port P1 Control (Determines either CMOS output or N-channel open drain output)

4.17.3 Differences of Pull-Up Control Register

Table 4.17.3 lists the differences of pull-up control register.

Table 4.17.3 Differences of Pull-Up Control Register

Symbol	Address		bit	Differences	
	M16C/62P	M32C/84		M16C/62P	M32C/84
PUR1	03FDh	03F1h	4	P6_0 to P6_3 Pull-Up	Nothing is assigned.
			5	P6_4 to P6_7 Pull-Up	Nothing is assigned.
			6	P7_2 to P7_3 Pull-Up	Nothing is assigned.
			7	P7_4 to P7_7 Pull-Up	Nothing is assigned.
PUR2	03FEh	03DAh	0	P8_0 to P8_3 Pull-Up	P6_0 to P6_3 Pull-Up
			1	P8_4 to P8_7 Pull-Up	P6_4 to P6_7 Pull-Up
			2	P9_0 to P9_3 Pull-Up	P7_2 to P7_3 Pull-Up
			3	P9_4 to P9_7 Pull-Up	P7_4 to P7_7 Pull-Up
			4	P10_0 to P10_3 Pull-Up	P8_0 to P8_3 Pull-Up
			5	P10_4 to P10_7 Pull-Up	P8_4 to P8_7 Pull-Up
			6	Nothing is assigned.	P9_0 to P9_3 Pull-Up
			7	Nothing is assigned.	P9_4 to P9_7 Pull-Up
PUR3	03DFh	03DBh	0	P11_0 to P11_3 Pull-Up	P10_0 to P10_3 Pull-Up
			1	P11_4 to P11_7 Pull-Up	P10_4 to P10_7 Pull-Up
			2	P12_0 to P12_3 Pull-Up	P11_0 to P11_3 Pull-Up
			3	P12_4 to P12_7 Pull-Up	P11_4 Pull-Up
			4	P13_0 to P13_3 Pull-Up	P12_0 to P12_3 Pull-Up
			5	P13_4 to P13_7 Pull-Up	P12_4 to P12_7 Pull-Up
			6	P14_0 and P14_1 Pull-Up	P13_0 to P13_3 Pull-Up
			7	P11 to P14 Enabling	P13_4 to P13_7 Pull-Up
PUR4	-	03DCh	-	-	Only M32C/84

4.17.4 Function Select Register

M32C/84 has the Function Select Registers (PSC, PSC2, PSC3, PSD1, PSL0 to PSL3, PS0 to PS3, PS5, PS8, and PS9). When multiple peripheral function outputs are assigned to a pin, set these function select registers to select which function is used.

4.17.5 Input Function Select Register

M32C/84 has the input function select registers (IPS and IPSA) which select input function.

4.18 Differences of Flash Memory

4.18.1 Differences of Flash Memory

Table 4.18.1 lists the differences of flash memory. Addresses of flash memory associated SFR are different in M16C/62P and M32C/84.

Table 4.18.1 Differences of Flash Memory

Symbol	Address		bit	Differences	
	M16C/62P	M32C/84		M16C/62P	M32C/84
FIDR	01B4h	-	-	Only M16C/62P	-
FMR0	01B7h	0057h	-	Different address	
FMR1	01B5h	0055h	-	Different address	

4.19 Peripheral Functions added in M32C/84

Peripheral Functions added in M32C/84 are as below.
- Intelligent I/O
- CAN
- DMACII
- X/Y Conversion

4.20 Differences of Development Tool

Table 4.20.1 lists the differences of development tool.

Table 4.20.1 Differences of Development Tool.

Tool	For M16C/62P	For M32C/84
C Compiler (including Simulator Debugger)	M3T-NC30WA	M3T-NC308WA
Real-time OS	M3T-MR30/4	M3T-MR308/4
Emulator Debugger	M16C R8C PC7501 M16C PC4701	M32C PC7501
Emulation Probe Emulation Pod	M3062PT2-EPB (for PC7501) M3062PT3-RPD-E (for PC4701)	M30850T2-EPB
Compact Emulator	M3062PT3-CPE	M30850T3-CPE
Renesas Starter Kits	R0K33062PS000BE	R0K330879S000BE

5. Reference Documents

Hardware manual

M16C/62P Group Hardware Manual

M32C/84 Group Hardware Manual

(Use the latest information on the home page: http://www.renesas.com)

TECHNICAL UPDATE/TECHNICAL NEWS

(Use the latest information on the home page: http://www.renesas.com)

Web site and Contact for Support

Renesas Technology Web site
http://www.renesas.com/

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http://www.renesas.com/inquiry
csc@renesas.com

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